In the Claims

Please amend the claims as follows:

1. (Original) A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

2. (Original) The memory of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer separating the polysilicon floating gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

3. (Original) The memory of claim 1, wherein the control gate includes a polysilicon control gate having a metal layer separating the polysilicon control gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

4. (Original) The memory of claim 1, wherein the gate oxide includes silicon dioxide having a tunnel barrier height of about 3.2 eV.

5. (Original) The memory of claim 1, wherein the metal oxide insulator includes a transition metal oxide.

6. (Original) The memory of claim 1, wherein the metal oxide insulator includes aluminum oxide.

7. (Original) The memory of claim 1, wherein the metal oxide insulator includes lead oxide.

8. (Original) The memory of claim 1, wherein the metal oxide insulator includes zirconium oxide.

9. (Original) The memory of claim 1, wherein the metal oxide insulator includes titanium oxide.

10. (Original) The memory of claim 1, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

11. (Original) The memory of claim 1, wherein the channel region includes an n-type channel.

12. (Original) A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate;

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

a first metal layer separating the metal oxide insulator and the floating gate, the first metal layer in contact with the floating gate;

a second metal layer separating the metal oxide insulator and the control gate, the metal layer in contact with the control gate, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

13. (Original) The memory of claim 12, wherein the control gate is a vertical control gate.

14. (Original) The memory of claim 13, wherein the control gate is a polysilicon edge defined vertical control gate.

15. (Original) The memory of claim 12, wherein the memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

16. (Original) The memory of claim 12, wherein the metal oxide insulator includes a transition metal oxide.

17. (Original) The memory of claim 12, wherein the metal oxide insulator includes aluminum oxide.

18. (Original) The memory of claim 12, wherein the metal oxide insulator includes niobium oxide.

19. (Original) The memory of claim 12, wherein the metal oxide insulator includes tantalum oxide.

20. (Original) The memory of claim 12, wherein the floating gate includes a horizontally oriented floating gate in contact with the gate oxide.

21. (Original) The memory of claim 12, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV, the floating gate includes polysilicon, and the control gate includes polysilicon.

22. (Original) A memory comprising:

an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide including silicon oxide having a tunneling barrier height of about 3.2 eV;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a tunneling barrier height less than the tunneling barrier height of the silicon oxide;

a number of bit lines coupled to the source regions along a first direction in the array of memory cells; and

a number of word lines coupled to the control gates along a second direction in the array of memory cells, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

23. (Original) The memory of claim 22, wherein each memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

24. (Original) The memory of claim 22, wherein each memory cell further includes a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in

contact with the metal oxide insulator, and a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

25. (Original) The memory of claim 24, wherein the floating gate includes polysilicon, the first metal layer contacting the floating gate, and the control gate includes polysilicon, the second metal layer contacting the control gate.

26. (Original) The memory of claim 25, wherein the metal oxide insulator includes a metal oxide insulator having a tunneling barrier height of less than 2 eV.

27. (Original) The memory of claim 26, wherein the control gate is a polysilicon edge defined vertical control gate.

28. (Original) The memory of claim 25, wherein the metal oxide insulator includes a transition metal oxide.

29. (Original) The memory of claim 25, wherein the metal oxide insulator includes aluminum oxide.

30. (Original) The memory of claim 25, wherein the metal oxide insulator includes lead oxide.

31. (Original) The memory of claim 25, wherein the metal oxide insulator includes zirconium oxide.

32. (Original) The memory of claim 25, wherein the metal oxide insulator includes niobium oxide.

33. (Original) The memory of claim 25, wherein the metal oxide insulator includes tantalum

oxide.

34. (Original) The memory of claim 25, wherein the metal oxide insulator includes titanium oxide.

35. (Original) The memory of claim 25, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

36-109. (Canceled)

110. (Previously Presented) An electronic system comprising:

a processor; and

a memory coupled to the processor, wherein the memory includes an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

111. (Previously Presented) The electronic system of claim 110, wherein each memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the

non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

112. (Previously Presented) The electronic system of claim 110, wherein the control gate is a vertical control gate.

113. (Previously Presented) The electronic system of claim 110, wherein the vertical control gate is a polysilicon edge defined vertical control gate.

114. (Previously Presented) The electronic system of claim 110, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV.

115. (Previously Presented) The electronic system of claim 110, wherein the metal oxide insulator includes a transition metal oxide.

116. (Previously Presented) The electronic system of claim 110, wherein the metal oxide insulator includes aluminum oxide.

117. (Previously Presented) The electronic system of claim 110, wherein the metal oxide insulator includes lead oxide.

118. (Previously Presented) The electronic system of claim 110, wherein the metal oxide insulator includes tantalum oxide.

119. (Previously Presented) The electronic system of claim 110, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

120. (Previously Presented) An electronic system comprising:

a processor; and

a memory coupled to the processor, wherein the memory includes:

an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate;

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; and

a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in contact with the metal oxide insulator;

a number of bit lines coupled to the source regions along a first direction in the array of memory cells; and

a number of word lines coupled to the control gates along a second direction in the array of memory cells, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

121. (Previously Presented) The electronic system of claim 120, wherein each memory cell further includes a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

122. (Previously Presented) The electronic system of claim 121, wherein the floating gate includes polysilicon, the first metal layer contacting the floating gate, and the control gate includes polysilicon, the second metal layer contacting the control gate.

123. (Previously Presented) The electronic system of claim 122, wherein the gate oxide

includes silicon oxide having a tunneling barrier height of about 3.2 eV.

124. (Previously Presented) The electronic system of claim 123, wherein the metal oxide insulator includes zirconium oxide.

125. (Previously Presented) The electronic system of claim 122, wherein the metal oxide insulator includes a transition metal oxide.

126. (Previously Presented) The electronic system of claim 122, wherein the metal oxide insulator includes zirconium oxide.

127. (Previously Presented) The electronic system of claim 122, wherein the metal oxide insulator includes niobium oxide.

128. (Currently Amended) The electronic system of claim 122, wherein the metal oxide insulator includes titanium ~~oxide~~ oxide.

129. (Previously Presented) The electronic system of claim 122, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

130. (Previously Presented) A method of forming a memory, comprising:

forming a memory cell including:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to one of the source and drain regions;

forming a gate oxide on the channel region, the gate oxide having a first tunneling barrier height;

forming a floating gate opposing the channel region, the floating gate separated from the channel region by the gate oxide;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; and

adapting the memory to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

131. (Previously Presented) The method of claim 130, wherein forming a metal oxide insulator includes forming a transition metal oxide insulator.

132. (Previously Presented) The method of claim 130, wherein forming a metal oxide insulator includes forming aluminum oxide.

133. (Previously Presented) The method of claim 130, wherein forming a metal oxide insulator includes forming zirconium oxide.

134. (Previously Presented) The method of claim 130, wherein forming a metal oxide insulator includes forming lead oxide.

135. (Previously Presented) The method of claim 130, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

136. (Previously Presented) The method of claim 130, wherein forming a floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the metal oxide insulator.

137. (Previously Presented) The method of claim 130, wherein forming a control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the metal oxide insulator.

138. (Previously Presented) The method of claim 130, wherein forming a gate oxide includes forming silicon dioxide having a tunneling barrier height of about 3.2 eV.

139. (Previously Presented) The method of claim 130, wherein forming a control gate includes forming an edge defined vertical control gate.

140. (Previously Presented) A method of forming a memory, comprising:

forming an array of memory cells, wherein forming each memory cell includes:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to the drain region;

forming a floating gate opposing the channel region;

forming a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

forming a first metal layer separating the metal oxide insulator and the floating gate, the first metal layer in contact with the floating gate;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

forming a number of bit lines coupled to the source regions along a first direction in the array of memory cells;

a number of word lines coupled to the control gates along a second direction in the array of memory cells; and

adapting the memory to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

141. (Previously Presented) The method of claim 140, wherein adapting the memory to operate each memory cell includes adapting the memory to control each memory cell to access a

first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode, wherein the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

142. (Previously Presented) The method of claim 140, wherein the method further includes forming a second metal layer on the control gate, the second metal layer in contact with the metal oxide insulator.

143. (Previously Presented) The method of claim 142, wherein forming a floating gate includes forming a polysilicon floating gate.

144. (Previously Presented) The method of claim 143, wherein forming a gate oxide includes forming silicon oxide having a tunneling barrier height of about 3.2 eV.

145. (Previously Presented) The method of claim 144, wherein forming a metal oxide insulator includes forming a transition metal oxide.

146. (Previously Presented) The method of claim 144, wherein forming a metal oxide insulator includes forming titanium oxide.

147. (Previously Presented) The method of claim 144, wherein forming a metal oxide insulator includes forming tantalum oxide.

148. (Previously Presented) The method of claim 144, wherein forming a metal oxide insulator includes forming niobium oxide.

149. (Previously Presented) The method of claim 144, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

150. (Previously Presented) The method of claim 144, wherein forming a source region and a drain region includes forming a n+ source region and a n+ drain region.

151. (Currently Amended) The method of claim 144, wherein [[the]] forming a control gate ~~lines~~ includes forming a ~~forming a~~ vertical control gate.

152. (Currently Amended) The method of claim 144, wherein [[the]] forming a control gate ~~lines~~ includes ~~forming a~~ forming an edge defined vertical control gate.

153. (Previously Presented) A method of forming an electronic system, comprising:

providing a processor; and

coupling the processor to a memory, the memory formed by a method including:

forming a memory cell, the memory cell formed by:

forming a source region and a drain region separated by a channel region in a substrate;

forming a storage capacitor coupled to one of the source and drain regions;

forming a gate oxide on the channel region, the gate oxide having a first tunneling barrier height;

forming a floating gate opposing the channel region, the floating gate separated from the channel region by the gate oxide;

forming a control gate opposing the floating gate; and

forming a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; and

adapting the memory to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

154. (Previously Presented) The method of claim 153, wherein adapting the memory to

operate the memory cell includes adapting the memory to control the memory cell to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode, wherein the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

155. (Previously Presented) The method of claim 153, wherein the method further includes forming a first metal layer on the floating gate, the first metal layer in contact with the metal oxide insulator.

156. (Previously Presented) The method of claim 155, wherein forming a gate oxide includes forming silicon dioxide having a tunneling barrier height of about 3.2 eV.

157. (Previously Presented) The method of claim 156, wherein forming a floating oxide includes forming a polysilicon floating gate and forming a control gate includes forming a polysilicon control gate.

158. (Previously Presented) The method of claim 155, wherein the method further includes forming a second metal layer on the control gate, the second metal layer in contact with the metal oxide insulator.

159. (Previously Presented) The method of claim 155, wherein forming a metal oxide insulator includes forming a transition metal oxide insulator.

160. (Previously Presented) The method of claim 155, wherein forming a metal oxide insulator includes forming aluminum oxide.

161. (Previously Presented) The method of claim 155, wherein forming a metal oxide insulator includes forming zirconium oxide.

162. (Previously Presented) The method of claim 155, wherein forming a metal oxide insulator includes forming lead oxide.

163. (Previously Presented) The method of claim 155, wherein forming a metal oxide insulator includes forming a Perovskite metal oxide insulator.

164. (Previously Presented) A method comprising:

operating a memory adapted to control a memory cell in a volatile memory mode and in a non-volatile memory mode, the memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

sensing a first charge representing a data value from the storage capacitor if the memory operates the memory cell in the volatile memory mode; and

sensing a second charge representing a data value from the floating gate if the memory operates the memory cell in the volatile memory mode.

165. (Previously Presented) The method of claim 164, wherein the method further includes writing to the floating gate using channel hot electron injection.

166. (Previously Presented) The method of claim 165, wherein writing to the floating gate using channel hot electron injection includes:

applying a large voltage to the control gate; and

applying a large voltage to the drain region.

167. (Previously Presented) The method of claim 164, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

168. (Previously Presented) The method of claim 167, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

169. (Previously Presented) The method of claim 164, wherein the method further includes erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate.

170. (Previously Presented) The method of claim 169, wherein erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

171. (Previously Presented) The method of claim 169, wherein tunneling electrons from the floating gate to the control gate includes tunneling electrons from a first metal layer formed on the floating gate through the metal oxide insulator to a second metal layer formed on the control gate, the first metal layer in contact with the metal oxide insulator and the second metal layer in contact with the metal oxide insulator.

172. (Previously Presented) The method of claim 164, wherein the method further includes reading the memory cell in the non-volatile memory mode by:

applying a positive voltage to the control gate of the memory cell; and

sensing a current from the drain region.

173. (Previously Presented) The method of claim 164, wherein operating the memory to control the memory cell in the volatile memory mode includes reading charge from the capacitor of the memory cell and/or writing charge from the capacitor of the memory cell.

174. (Previously Presented) A method comprising:

operating a memory adapted to control a memory cell in a volatile memory mode and in a non-volatile memory mode, the memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a polysilicon floating gate opposing the channel region, the polysilicon floating gate having a metal layer disposed thereon;

a silicon oxide layer separating the floating gate from the channel region, the silicon oxide layer having a tunneling barrier height of about 3.2 eV;

a metal oxide insulator, the metal oxide insulator having a tunneling barrier height being less than the tunneling barrier height of the silicon oxide layer, the metal oxide insulator in contact with the metal layer disposed on the polysilicon floating gate; and

a control gate opposing the floating gate and separated from the floating gate by the metal oxide insulator; and

sensing a first charge representing a data value from the storage capacitor if the memory operates the memory cell in the volatile memory mode; and

sensing a second charge representing a data value from the floating gate if the memory operates the memory cell in the volatile memory mode.

175. (Previously Presented) The method of claim 174, wherein the method further includes writing to the floating gate using channel hot electron injection.

176. (Previously Presented) The method of claim 175, wherein writing to the floating gate using channel hot electron injection includes:

applying a large voltage to the control gate; and

applying a large voltage to the drain region.

177. (Previously Presented) The method of claim 174, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

178. (Previously Presented) The method of claim 177, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

179. (Previously Presented) The method of claim 174, wherein the method further includes erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate.

180. (Previously Presented) The method of claim 179, wherein erasing charge from the floating gate by tunneling electrons from the floating gate to the control gate includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

181. (Previously Presented) The method of claim 179, wherein tunneling electrons from the floating gate to the control gate includes tunneling electrons from the metal layer disposed on the floating gate through the metal oxide insulator to a metal layer disposed on the control gate, the metal layer disposed on the control gate in contact with the metal oxide insulator, the control gate including polysilicon.

182. (Previously Presented) The method of claim 174, wherein the method further includes reading the memory cell in the non-volatile memory mode by:

applying a positive voltage to the control gate of the memory cell; and

sensing a current from the drain region.

183. (Previously Presented) The method of claim 174, wherein operating the memory to control the memory cell in the volatile memory mode includes reading charge from the capacitor of the memory cell and/or writing charge from the capacitor of the memory cell.